vtool smart verification

Rule The Bugs

Vtool is a comprehensive UVM functional verification platform that shortens the ever increasing ASIC and FPGA verification cycle, by providing an efficient, reusable, and maintainable verification environment.

machina

The perfect solution for building your verification environment

Easily and quickly build or import UVCs and create UVM testbenches.

Visually create what you can, and code only what you need, in a two-way process that synchronizes GUI with UVM code.

Machina automatically maintains a fully documented and beautifully structured code, ensuring clear readability and high reusability.

Let Machina handle UVM complexity and integration, while you focus on the real work of core verification.

vitalitas

The optimal solution for creating your sequences and tests

Create complex graph-based sequences and tests, by positioning actions on a flowchart that sets in motion the entire verification stimuli.

Vitalitas utilizes fully configurable standard functions, including loops, forks, logic statements, registers access, nested sequences, UVM messages, events, and custom created code.

Let Vitalitas bypass huge UVM files, providing you with a sequence library that is easy to create, simple to maintain, and clear to understand.

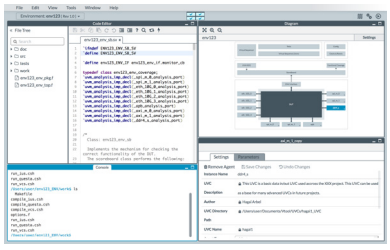
cogita

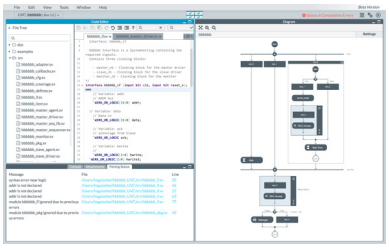
The ultimate solution for pinpointing and blasting bugs

Analyze the log file in an innovative visual representation, intuitively revealing key data patterns.

Cogita runs clever search-and-match string patterns, to efficiently display and pinpoint buggy test scenarios.

Let Cogita bug hunt via log file visual analysis, telling you the story behind the scenarios and instantly revealing all bugs.





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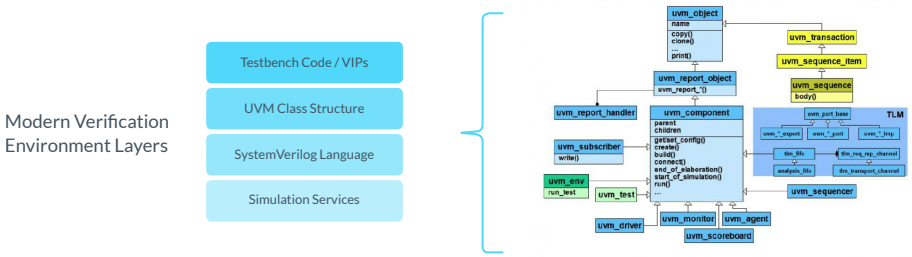
Why Vtool

Today, an average of 70% of the IC development process is focused on verification, most of which is spent on testbench development and debug. This has lead to an evolution of testbench techniques, the latest of which is Accellera's Unified Verification Methodology (UVM) standard. Although these techniques provide effective verification solutions, developing modern environments is complex, error prone, and time consuming. Solutions, such as UVM subsets, template schemes, and IDE extensions are inflexible and do not improve the core issues of comprehension, creation and management of the millions of lines of testbench code.



Meeting Modern Verification Challenges

The unique Vtool approach solves real world, critical verification challenges:

Classic Verification Issues	Vtool Environment
Incomplete spec, unavailable DUT	Incremental development capability
Reuse code match issues	Reuse through library function
Verification code debug complexity	Simplified code visualization & creation
Expert required for core modeling	Easy to employ for UVM novice
Designers unable to assist in testing	Designers understand testbench
Ramp up on unintelligible, old code	Load in old code, visualize structure
Documentation out of sync	Automated documentation generation
Templating schemes inflexible	Code regeneration enables flexibility

Recent User Quote:

"Vtool allowed us to accomplish in days what it would have otherwise taken weeks. We appreciated its effectiveness, friendliness and ease of use."

JG, verification manager

Comments from Engineering Team Working On SoC Device

- Large platorm IC, significant verification effort
  "Vtool has improved verification productivity by 50%"
- Full chip integration usually requires 3-4 weeks
  "With Vtool same point reached in 1 day"
- Creation APB UVC incl. debug, coverage, docs: 3 weeks
  "With Vtool task performed in 1 day"

About Vtool

Established in 2014, Vtool is headquartered in Israel and has offices around the globe. Spun out of the successful Veriest Consulting company, it's solutions have been developed over the last four years, based on real-world, practical verification projects.

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