NEWS RELEASE

Vtool Introduces Cogita™, Next-Generation, Verification Debug Solution Leveraging Advanced Visualization and Machine Learning

Cogita Already Accelerating Verification Team's Complex Debug Processes Up To An Order-of-Magnitude Over Traditional Signal-Level Analysis

SAN JOSE, CALIF. –– February 19, 2019 –– Vtool, the leading verification and debug innovator today introduced the full production version of Cogita, a powerful new semiconductor verification debug solution.

Cogita leverages advanced visualization structures, Machine Learning algorithms, and unified data sources to accelerate the discovery of the root causes of design bugs. Already in use today at multiple leading electronic system and semiconductor companies, the solution has been shown to accelerate debug from 5-10X over traditional, signal-level solutions on complex designs.

"While semiconductor verification has seen explosive evolution, debug has barely changed over the last 25 years," noted Hagai Arbel, Chief Executive Officer at Vtool. "Cogita will revolutionize debug as we know it by leveraging visual abstraction, machine learning and advanced use models to allow engineers to track through the debug process quickly and accurately."

The Cogita Difference
In today's methodical, iterative debug processes, low-level signals are examined step-by-step, assumptions are validated using verbose log and wave data, and engineers examine multiple error condition possibilities before hitting the right one. This meticulous methodology is time-consuming and error-prone, yielding sub-standard results.

Cogita applies advanced visualization techniques and powerful machine learning algorithms to give the engineer a new perception of the entire design and verification scenario. Applying automation in an ergonomically fashioned solution, bug causes are revealed rapidly and effectively. A configurable parser reads log and waveform files into an advanced database. The engineer, working from an abstract perspective, performs educated search queries leveraging graphical "players". Machine learning is used to classify information, enabling smart decisions that lead rapidly to the root cause of issues.

The solution appears particularly useful for large-scale emulation environments, as well as simulation, whereby reducing the data needed over traditional approaches and observing the verification run from an abstract level, bugs can be fixed quickly without the need to rerun lower-level simulation and perform other testing. Cogita works with existing emulation and simulation environments and cooperates hand-in-hand with existing debug solutions to accelerate the overall use models.

Cogita is in use today by multiple verification teams. They have found that they can accelerate their debug processes up to an order-of-magnitude to dramatically reduce schedule and resource needs, apply advanced visualization for a clear understanding of designs and tests to increase verification quality & coverage, and leverage the solution on large-scale emulation/simulation runs to streamline the analysis of the toughest corner-cases.

Availability and Pricing
Cogita is in full-volume production now. Pricing is available upon request.

A white paper on the new technology are available on the Vtool website: thevtool.com.

Cogita will be demonstrated in the Vtool booth (#901) during DVCon Monday, February 25, through Wednesday, February 27, at the DoubleTree Hotel in San Jose, Calif.

Vtool will also co-sponsor the Verification 3.0 Innovation Summit on Tuesday, March 19, at the Levi Stadium Conference Center in Santa Clara, Calif.

About Vtool
Based in Tel Aviv, Israel, Vtool is a privately held EDA company that develops, markets and licenses advanced verification products developed by leading verification engineers. Vtool has offices in Tel Aviv, Belgrade, Serbia with direct sales in Europe and sales representation in Japan and North America. The Vtool solution is a comprehensive visual UVM functional verification and advanced debug platform that shortens the ever-increasing ASIC and FPGA verification cycle, by providing an efficient, reusable, and maintainable verification environment. For more information visit www.thevtool.com.

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